

# LM26LV Evaluation Board User's Guide



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#### References

1. "LM26LV 1.6V, LLP-6, Factory Preset Temperature Switch and Temperature Sensor" datasheet.

The latest copy of the **LM26LV** datasheet can be obtained by going to the National Semiconductor website<u>www.national.com</u>, by searching on "**LM26LV**", and then downloading the **LM26LV**.pdf file.

#### 1.0 Introduction

The LM26LV Evaluation Board offers the user a convenient way to experiment with the operation of the LM26LV Temperature Switch and Temperature Sensor.

There are jumpers that allow the insertion of an output series resistor, the measurement of IDD, and the selection of the TRIP TEST mode.

By default, jumpers J3 (IDD) and J4 (VOUT) are installed. Resistor R3 can be installed and J4 removed to insert it in series with the output. See the datasheet for recommended values for R3. By default J2

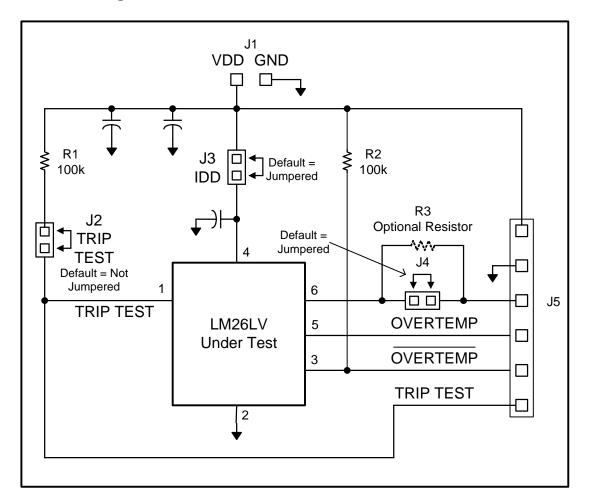
is left open but a jumper is provided so that the user can use the TRIP TEST mode.

Note that R1 is only in the circuit for protection. This resistor is not required in actual operation. The TRIP TEST Pin can be connected directly to VDD to select the TRIP TEST Mode.

R2, the pull-up resistor for the open-drain output OVERTEMP#, is 100k on the board. See the datasheet for more details about this value. If this pin is not used by the customer it may be left open.

The block diagram below shows the jumpers in the default condition.

# 1.1 Block Diagram



#### 2.0 Quick Start

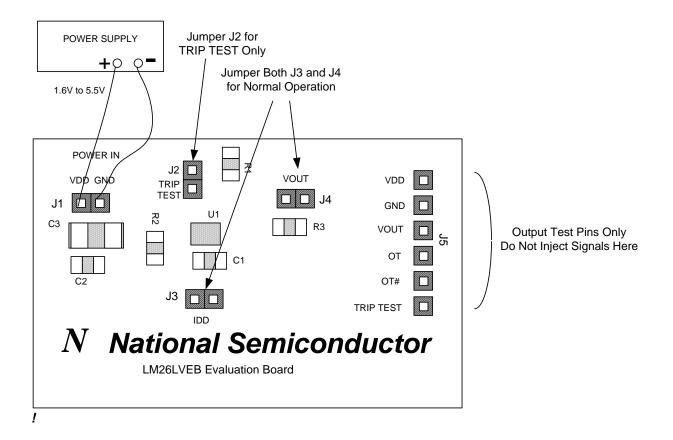
The diagram below shows how the LM26LV is connected in a typical bench test configuration.

Before applying power directly to the LM26LV Evaluation Board, make sure that the voltage is between +1.6 VDC and +5.5 VDC. Also make sure that J3 and J4 are

jumpered for normal operation. Jumpering J2 will put the LM26LV in TRIP TEST mode, not for normal operation.

Apply power to the LM26LV evaluation board. Measure the output voltage connected between to output pin (J4) and ground for the VTEMP Output voltage.

#### 2.1 Quick Start Diagram



# 3.0 Functional Description

See the details of the normal operation and the TRIP TEST mode operation in the datasheet.

See the datasheet for details regarding the VTEMP inversely proportional output voltage vs temperature characteristic.

# 3.1 LM26LVEB Evaluation Board Connection Table

Connector Label	Connector Name	Pin Number	Description
T1	POWER IN	1	VDD Supply +1.6 to 5.5 VDC to this pin.
J1 POWER IN	POWEK IN	2	GND This is Power Supply return for V <sub>DD</sub> Input
J2 TRIP TEST	TDID TEST	1 -2	If pins 1 and 2 are jumpered then TRIP TEST
	TRIP TEST		Mode is selected.
J3 IDD			Jumper is installed unless a milliammeter is used
			to measure the actual IDD.
J4 VOUT Output			Jumper is installed across pins 1 and 2 by default.
J4	V <sub>OUT</sub> Output		Otherwise resistor R3 is in series with the output.
J5 Test Pins			Use these pins to test and monitor the signals on
J5	Test Pilis		the board. Do not inject signals here.

# 4.0 Electrical and Mechanical Specifications

# **4.1 Electrical Specifications**

Power Requirements	
The Board uses the +1.6 VDC to +5.5 VDC and GND lines from an external	+1.6 VDC to
low-noise power supply.	+5.5 VDC

# 4.2 Electrical Schematic

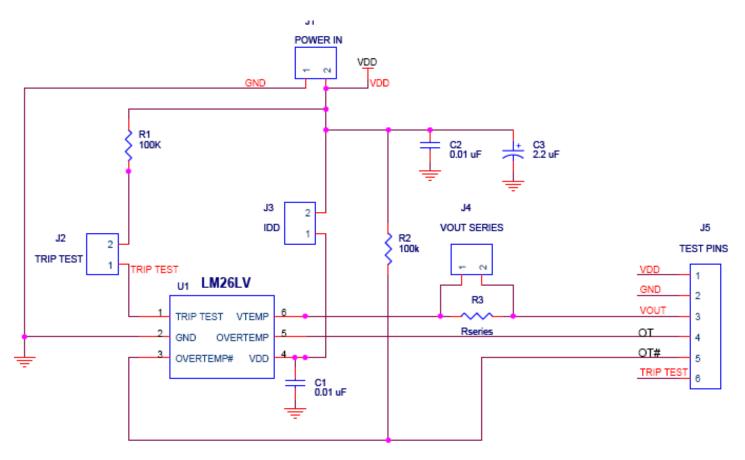


Figure 4.2 Schematic Diagram of the LM26LV Evaluation Board

# 4.3 Evaluation Board Layout

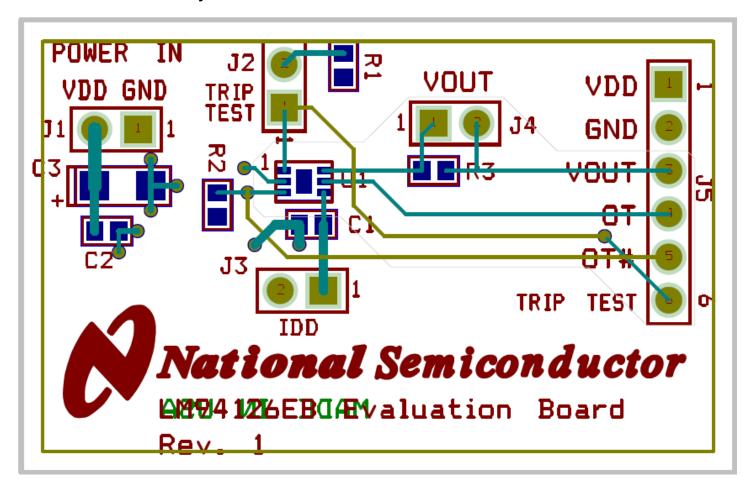


Figure 4.3 Layout diagram of the LM26LV Evaluation Board

#### 4.4 Bill of Materials for LM26LV Evaluation Board

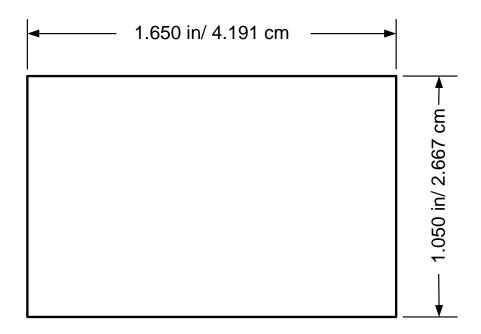
Item	Quantity	Reference	Part	
1	2	C1, C2	Capacitor, Ceramic, 0.01 uF	
2	1	C3	Capacitor Ceramic, 2.2 uF	
3	4	J1, J2, J3, J4	Header, 1X2, 0.1 in centers	
4	1	J5	Header, 1X6, 0.1 in centers	
6	2	R1, R2	Resistor, 100k	
7	1	R3	Resistor, (not stuffed)	
8	1	U1	LM26LVCISD Device Under Test (DUT)	
9	1		Circuit Board, Fabricated, LM26LVEB Evaluation Board, Rev. 1	

# 4.5 Mechanical Specifications

# 4.5.1 Operating Mechanical and Environmental Specifications

	Minimum	Typical	Maximum
Temperature	0°C	25°C	70°C

#### 4.5.2 Evaluation Board Basic Dimensions



# 4.5.3 Electrostatic Discharge (ESD) Precautions

The user shall use ESD precautions as specified in National Semiconductor ESD document (SC)CSI-3-038 available through www.national.com.

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